30454-122 (P-3605)

ABSTRACTS

A method of generating synthesis scripts to synthesize integrated circuit (IC) designs described in a generic netlist into gate-level description comprising the steps of identifying hardware elements in a generic netlist, determining key pins for each of

5   said identified hardware elements, extracting design structure and hierarchy from the Generic netlist, generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design, generating script to cause a logic synthesis tool to apply top-down characterization to modules and sub-modules of the IC design and generating script to cause a logic synthesis tool to repeat said

10   bottom-up and said top-down applications until constraints are satisfied.

141